$SrTiO_3$ (STO) on Silicon

Thin $SrTiO_3$ film deposited on top of a doped Si substrate.

PROPERTIES

Size	5x5, 10x10, 15x15 mm² (other shapes available on request)
Thickness	725 ± 25 µm
Orientation	(001) ± 0.5°
Doping	p-type
Resistivity	1-30 Ωcm
SrTiO3 layer	4.0 ± 0.2 nm
Roughness	3 ± 2 Å
Mosaicity	0.4°
Max temp.	800°C

USE CASES:

- Projects on oxide epitaxy with perovskites (ferroelectrics, multiferroics, colossal magnetoresistance, high-Tc superconductivity etc.)
- Larger surfaces possible compared to regular STO crystals
- Layer transfer (i.e., removing Si is easy, STO not)
- MEMS processes with oxides (fabrication of oxide membranes by underetching the Si substrate)

IDEAL FOR:

Researchers / R&D departments interested in oxide epitaxy with pervoskites (ferroelectrics, multiferroics, colossal magnetoresistance, high-Tc superconductivity, …) seeking to

- Scale up their technology (i.e., integration with Si is the only way forward)
- Get larger surfaces than what is possible with STO crystals
- Produce MEMS (via underetching of Si)
- Transfer layers of STO
- Use doped Si as backside contact layer (usually Nb doping for STO)

REFERENCES

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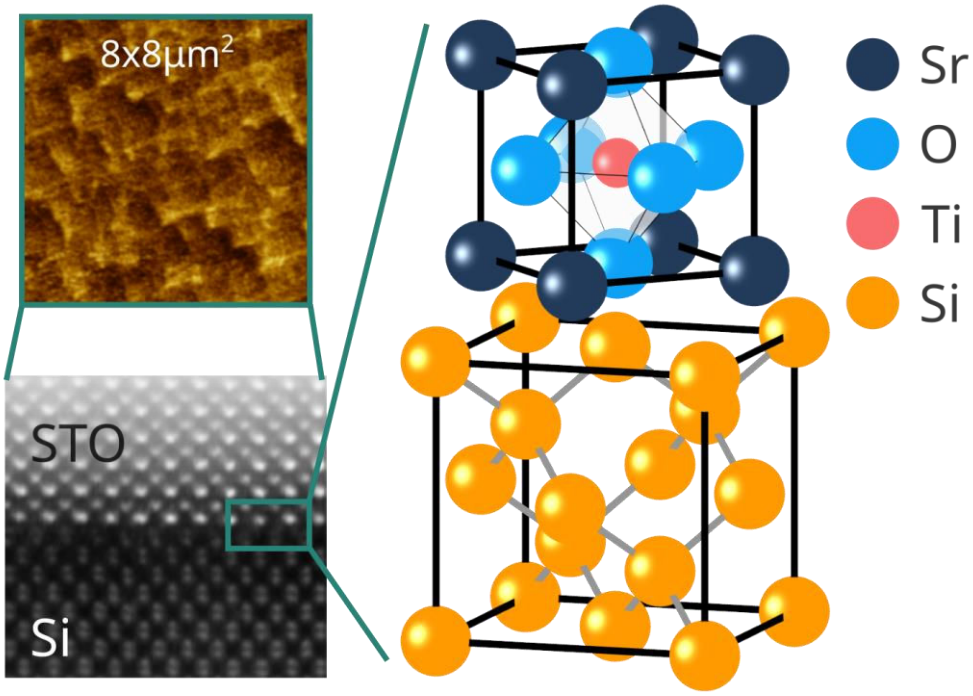
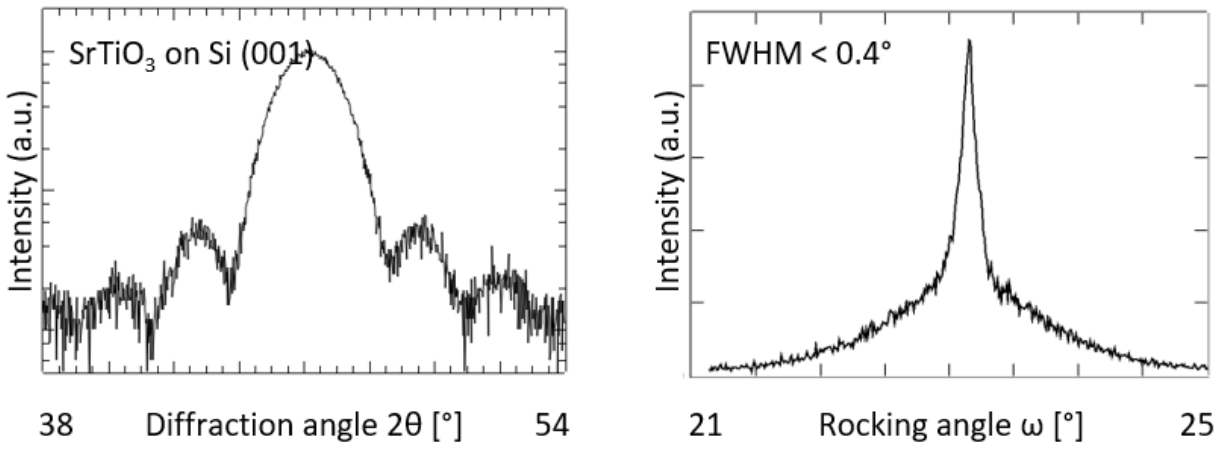


Bottom left: TEM image of the interface between Si substrate and STO apitaxial layer. Top left: 8x8 µm2 AFM image. The terraces have a height of ~2 Å. Right: Schematic of the crystal lattices with color coded atoms.



Left: XRD analysis of STO epitaxial layer on Si. Right: rocking curve demonstrating a mosacitiy < 0.4°